Amendments to Claims

Claim 1 (previously presented): A method of forming a transistor device, comprising:

exposing a substrate surface having a first peak nitrogen concentration to activated nitrogen to form an exposed surface having a second peak nitrogen concentration at least 15% (atom percent) greater than the first peak nitrogen concentration;

providing a channel region on one side of the exposed surface;

providing a transistor gate structure on a side of the exposed surface that is opposed to said one side; and

forming a pair of source/drain regions separated from one another by the channel region.

Claim 2 (previously presented): The method of claim 1 further comprising forming a layer of silicon dioxide over the channel region, and wherein the substrate surface comprises a surface of the silicon dioxide.

Claim 3 (original): The method of claim 1 wherein the transistor device is a PMOS device.

Claim 4 (original): The method of claim 1 wherein the transistor device is an NMOS device.

Claim 5 (currently amended): The method of claim 1 further comprising ~~subjecting~~ heating the exposed surface to ~~an anneal at~~ a temperature of about 900°C for a time of from about 10 seconds to about 60 ~~seconds; and~~ seconds, wherein the ~~exposed surface is heated to the anneal temperature by~~ heating comprises rapid thermal processing at a temperature ramp rate of at least about 10°C/second.

Claims 6-25 (canceled).

Claim 26 (previously presented): A method of forming a transistor device, comprising:

defining a channel region of the transistor device beneath a substrate surface;

implanting a dopant into the channel region to a concentration of less than about 7×10^{17} atoms/cm^3 as a V_t implant;

forming a dielectric material over the channel region, the forming the dielectric material comprising exposing the substrate surface to activated nitrogen to increase a peak nitrogen concentration within the substrate surface by at least about 15 atom percent, the dielectric material comprising the exposed surface;

forming a transistor gate structure over the dielectric material; and

forming a pair of source/drain regions separated from one another by the channel region.

Claim 27 (previously presented): The method of claim 26 further comprising forming a layer of silicon dioxide over the channel region, and wherein the substrate surface comprises the silicon dioxide.

Claim 28 (original): The method of claim 26 wherein the transistor device is a PMOS device.

Claim 29 (original): The method of claim 26 wherein the concentration of dopant in the V_t implant is less than 7×10^{17} atoms/cm^3.

Claim 30 (original): The method of claim 26 wherein the concentration of dopant in the V_t implant is from about 1×10^{17} atoms/cm^3 to 7×10^{17} atoms/cm^3.

Claim 31 (original): The method of claim 26 wherein the concentration of dopant in the V_t implant is from about 1×10^{17} atoms/cm^3 to 5×10^{17} atoms/cm^3.

Claim 32 (original): The method of claim 26 wherein the activated nitrogen is formed from a plasma maintained at a power of from about 1,500 watts to about 5,000 watts.

Claim 33 (previously presented): The method of claim 26 wherein the activated nitrogen is formed from a plasma that is remote relative to the substrate surface.

Claim 34 (previously presented): The method of claim 26 wherein the activated nitrogen is formed from a plasma that contacts the substrate surface.

Claim 35 (previously presented): The method of claim 26 further comprising maintaining the substrate surface at a temperature of from about 25°C to about 400°C during the exposing of the substrate surface to the activated nitrogen.

Claims 36-67 (canceled).